What is Claimed Is:

1. A method for synchronizing two of more graphics processing units, comprising:

determining whether the phase of a first timing signal of a first graphics processing unit and the phase of a second timing signal of a second graphics processing unit are synchronized; and

adjusting the frequency of the first timing signal to the frequency of the second timing signal if the first timing signal and the second timing signal are not synchronized.

2. The method of claim 1, further comprising transmitting the synchronized timing signal to a third graphics processing unit.

3. The method of claim 1, further comprising:

determining whether a first stereo field signal of the first graphics processing unit and a second stereo field signal of the second graphics processing unit are synchronized; and

adjusting the phase of the first stereo field signal to the phase of the second stereo field signal if the first stereo field signal and the second stereo field signal are not synchronized.

4. The method of claim 3, further comprising transmitting the synchronized stereo field signal to a third graphics processing unit.

5. The method of claim 1, further comprising synchronizing a swap ready signal of the first graphics processing unit with a swap ready signal of the second graphics processing unit.

6. The method of claim 5, wherein synchronizing the swap ready signal of the first graphics processing unit with the swap ready signal of the second graphics processing unit comprises:

receiving a frame divider;

triggering a new video start address in a memory; and

determining whether a swap ready element on at least one of the graphics processing units is logically true.

7. The method of claim 6, further comprising scanning out data from the memory starting at the new video start address if the swap ready element on the at least one of the graphics processing units is logically true.

8. The method of claim 6, further comprising, prior to determining whether the swap ready element on the at least one of the graphics processing units is logically true:

determining whether the current scanline is within a video blanking interval; and

scanning out the data from the memory starting at the new video start address if the swap ready element on the at least one of the graphics processing units is logically true and the current scanline is within the video blanking interval.

9. The method of claim 6, further comprising performing a series of video memory block transfers if the swap ready element on the at least one of the graphics processing units is logically true.

10. The method of claim 6, further comprising, prior to determining whether the swap ready element on the at least one of the graphics processing units is logically true:

determining whether the current scanline is within a video blanking interval; and

performing the series of video memory block transfers if the swap ready element on the at least one of the graphics processing units is logically true and the current scanline is within the video blanking interval.

11. The method of claim 6, wherein the swap ready element is logically true when an image content stored in a back portion of a frame buffer in the at least one of the

graphics processing units is ready to be transferred to a front portion of the frame buffer.

12. The method of claim 6, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical HIGH state.

13. The method of claim 6, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical LOW state.

14. The method of claim 1, wherein the first graphics processing unit and the second processing unit are implemented on one of a silicon substrate, a printed circuit board, and an array of display elements.

15. A method for generating a synchronized timing signal in a graphics processing unit, comprising:

receiving a clock signal from a clock generator and an external synchronization signal;

determining whether the phase of the clock signal and the phase of the external synchronization signal are synchronized; and

adjusting the frequency of the clock generator to the frequency of the external synchronization signal if the clock signal and the external synchronization signal are not synchronized, thereby generating the synchronized timing signal.

16. The method of claim 15, further comprising transmitting the synchronized timing signal to a second graphics processing unit.

17. A method for scanning out data, comprising:

receiving a frame divider;

triggering a new video start address in a memory;

determining whether a swap ready element on at least one of two or more graphics processing units is logically true; and

scanning out data from the memory starting at the new video start address if the swap ready element on the at least one of the two or more graphics processing units is logically true.

18. The method of claim 17, further comprising suspending rendering in response to receiving the frame divider.

19. The method of claim 17, further comprising, prior to determining whether the swap ready element on the at least one of the two or more graphics processing units is logically true:

determining whether the current scanline is within a video blanking interval; and

scanning out the data from the memory starting at the new video start address if the swap ready element on the at least one of the two or more graphics processing units is logically true and the current scanline is within the video blanking interval.

20. The method of claim 17, wherein the swap ready element is logically true when an image content stored in a back portion of a frame buffer in the at least one of two or more graphics processing units is ready to be transferred to a front portion of the frame buffer.

21. The method of claim 17, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical HIGH state.

22. The method of claim 17, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical LOW state.

23. The method of claim 17, wherein the method is repeated for each frame.

24. A method for scanning out data, comprising:

receiving a frame divider;

determining whether a swap ready element on at least one of the two or more graphics processing units is logically true; and

performing a series of video memory block transfers if the swap ready element on the at least one of the two or more graphics processing units is logically true.

25. The method of claim 24, further comprising suspending rendering in response to receiving the frame divider.

26. The method of claim 24, further comprising, prior to determining whether the swap ready element on the at least one of the two or more graphics is logically true:

determining whether the current scanline is within a video blanking interval; and

performing the series of video memory block transfers if the swap ready element on the at least one of the two or more graphics processing units is logically true and the current scanline is within the video blanking interval.

27. The method of claim 24, wherein the swap ready element is logically true when an image content stored in a back portion of a frame buffer in the at least one of the two or more graphics processing units is ready to be transferred to a front portion of the frame buffer.

28. The method of claim 24, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical HIGH state.

29. The method of claim 24, wherein the swap ready element is logically true when a voltage on the swap ready element is in a logical LOW state.

30. The method of claim 24, wherein the method is repeated for each frame.

31. An apparatus for synchronizing two or more graphics processing units, comprising:

means for determining whether the phase of a first timing signal of a first graphics processing unit and the phase of a second timing signal of a second graphics processing unit are synchronized; and

means for adjusting the frequency of the first timing signal to the frequency of the second timing signal if the first timing signal and the second timing signal are not synchronized.

32. The apparatus of claim 31, further comprising:

means for determining whether a first stereo field signal of the first graphics processing unit and a second stereo field signal of the second graphics processing unit are synchronized; and

means for adjusting the phase of the first stereo field signal to the phase of the second stereo field signal if the first stereo field signal and the second stereo field signal are not synchronized.

33. The apparatus of claim 31, further comprising means for synchronizing a swap ready signal of the first graphics processing unit with a swap ready signal of the second graphics processing unit.